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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/022,826	12/20/2001	Sung-hee Hwang	1293.1215	1431

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EXAMINER	
TORRES, JOSEPH D	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 03/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/022,826	HWANG ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-8 and 32-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-8 and 32-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 1-3, 5-8 and 32-41 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-3, 5-8 and 32-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Noda; Chosaku (US 6175686 B1, hereafter referred to as Noda686) in view of Noda; Chosaku (US 6216245 B1, hereafter referred to as Noda245).

35 U.S.C. 103(a) rejection of claims 1 and 32.

Noda686 teaches encoding input data with an error correction code (ECC) to generate ECC encoded data in a plurality of ECC blocks, each ECC block having a predetermined size of rows and columns (Figure 6 in Noda686 is an ECC Block comprising 16 recording sectors identified by numbers 0 to 15; Figure 7 in Noda686 is a recording sector comprising 13x182 bytes, that is, an ECC Block is comprised of 16 recording sectors and labeled with identifiers 0-16; col. 12, lines 20-27 and Steps S207 and S208 of Figure 11 in Noda686 teaches that each channel A and B are error correction encoded to form two ECC blocks one for each channel, each ECC block comprised of 16 recording sectors and labeled with identifiers 0-16, that is, the ECC blocks for channel A and B are generated separately in an identical fashion as would be the ECC block of Figure 6 in the Standard Format, the channel A and B ECC blocks are standard format ECC blocks; Error Correction Processing block S208A generates the channel A standard format ECC block and Error Correction Processing block S208B generates the channel B standard format ECC block; see S208A and S208B in Figure 19 of Noda686 for details; col. 12, lines 39-49 in Noda686 teach that the channel A and B standard format ECC blocks of Figure 6 are arranged as in Figure 14 to form an extended error correction for which the channel A and B standard format ECC blocks form 2 extended ECC sub-blocks; col. 12, lines 39-49 in Noda686 teaches that each of the 2 extended ECC sub-blocks has its own inner and outer parity and, in fact, S208A and S208B in Figure 19 teach that ECC is generate separately and independently for each channel so that each extended ECC sub-block is an independent standard format ECC block; Note: in Figure 14, adjacent identifiers are of different standard format ECC

blocks, hence any Channel Synthesis unit for implementing block S211 in Figure 19 of Noda686 is an interleaver which extracts and arranges the identifiers from ones of the ECC blocks to generate a recording block such that adjacent identifiers are of different ECC blocks);

dividing each of the ECC blocks of the ECC encoded data further in row and column directions to form a plurality of partitions, each partition having a predetermined unit in row and column directions (Figure 6 in Noda686 teaches that each ECC block is partitioned into 16 rows and 182 byte-size columns; hence Noda686 teaches dividing each of the ECC blocks of the ECC encoded data further into 16 rows and and 185 byte-sized columns to form a plurality of partitions, each partition having a predetermined unit in row and column directions);

interleaving the data from the plurality of the partitions by alternately extracting data from the partitions of each of the ECC blocks so that partitions from each of the ECC blocks are alternately selected (col. 12, lines 39-49 in Noda686 teach that the channel A and B standard format ECC blocks of Figure 6 are arranged as in Figure 14 to form an extended error correction for which the channel A and B standard format ECC blocks form 2 extended ECC sub-blocks; col. 12, lines 39-49 in Noda686 teaches that each of the 2 extended ECC sub-blocks has its own inner and outer parity and, in fact, S208A and S208B in Figure 19 teach that ECC is generate separately and independently for each channel so that each extended ECC sub-block is an independent standard format ECC block; Note: in Figure 14, adjacent identifiers are of different standard format ECC blocks, hence any Channel Synthesis unit for

implementing block S211 in Figure 19 of Noda686 is an interleaver which extracts and arranges the identifiers from ones of the ECC blocks to generate a recording block such that adjacent identifiers are of different ECC blocks, hence; Noda686 teaches interleaving the data from the plurality of the partitions by alternately extracting data from the partitions of each of the ECC blocks so that partitions from each of the ECC blocks are alternately selected); modulating the first recording block (S213 in Figure 19 of Noda686); and recording the modulated first recording block on the optical disc (S213 in Figure 19 of Noda686).

However Noda686 does not explicitly teach the specific use of progression through the partitions of each ECC block occurs diagonally to generate a first recording block.

Noda245, in an analogous art, teaches use of progression through the partitions of each ECC block occurs diagonally to generate a first recording block.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Noda686 with the teachings of Noda245 by including use of progression through the partitions of each ECC block occurs diagonally to generate a first recording block. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of progression through the partitions of each ECC block occurs diagonally to generate a first recording block would have provided a means for efficient use of memory (col. 2, lines 39-48 in Noda245).

35 U.S.C. 103(a) rejection of claims 2 and 3.

Figure 6 in Noda245 teaches that the last 16 rows of outer code parity in Figure 5 are rearranged so that the rows are interleaved into the 13^{th} row of each sector.

35 U.S.C. 103(a) rejection of claim 5.

Col. 1, lines 49-55 in Noda245 teaches dividing each of the ECC blocks in a column direction by a predetermined number of bytes into object blocks; and dividing each of the object blocks in at least one of a row direction and the column direction by the predetermined number of bytes to generate the plurality of partitions for the purposes Reed-Solomon encoding of an ECC block.

35 U.S.C. 102(e) rejection of claim 6.

All of the data is interleaved using the algorithm of Figures 8 and 9 in Noda245.

35 U.S.C. 103(a) rejection of claim 7.

Figures 8 and 9 in Noda245 teach a predetermined number of bytes of the data are extracted and rearranged to generate the first recording block.

35 U.S.C. 103(a) rejection of claim 8.

Col. 1, lines 49-55 in Noda245 teach dividing each of the ECC blocks in a column direction by a predetermined number of bytes into object blocks; and dividing each of the object blocks in at least one of a row direction and the column direction by the

predetermined number of bytes to generate the plurality of partitions for the purposes Reed-Solomon encoding of an ECC block.

35 U.S.C. 103(a) rejection of claim 33.

Noda teaches dividing each of a plurality of error correction code (ECC) blocks into a plurality of partitions (Figure 5 in Noda245 teaches dividing each of a plurality of error correction code (ECC) blocks into 16 sector partitions); and interleaving the data from the partitions so that each of the ECC blocks is alternately and equally selected to generate a first recording block (Figure 8 in Noda245 teaches interleaving the data from the sector partitions so that each of the ECC blocks is delayed and alternately and equally selected to generate first recording blocks depicted in the rows of Figure 9 in Noda245).

35 U.S.C. 103(a) rejection of claim 34.

See Error Correction Encoder 3 in Figure 3 of Noda245.

35 U.S.C. 103(a) rejection of claim 35.

See Figure 7 in Noda245.

35 U.S.C. 103(a) rejection of claims 36 and 37.

Col. 1, lines 49-55 in Noda245 teach dividing each of the ECC blocks in a column direction by a predetermined number of bytes into object blocks; and dividing each of

the object blocks in at least one of a row direction and the column direction by the predetermined number of bytes to generate the plurality of partitions for the purposes Reed-Solomon encoding of an ECC block.

35 U.S.C. 103(a) rejection of claims 38 and 39.

Col. 1, lines 49-55 in Noda245 teach dividing each of the ECC blocks in a column direction by a predetermined number of bytes into object blocks; and dividing each of the object blocks in at least one of a row direction and the column direction by the predetermined number of bytes to generate the plurality of partitions for the purposes Reed-Solomon encoding of an ECC block.

35 U.S.C. 103(a) rejection of claim 40.

Modulation Section 4 in Figure 3 of Noda245 is a means for modulating the first recording block; and recording the modulated first recording block on the optical disc.

35 U.S.C. 103(a) rejection of claim 41.

Col. 14, lines 50-53 in Noda686.

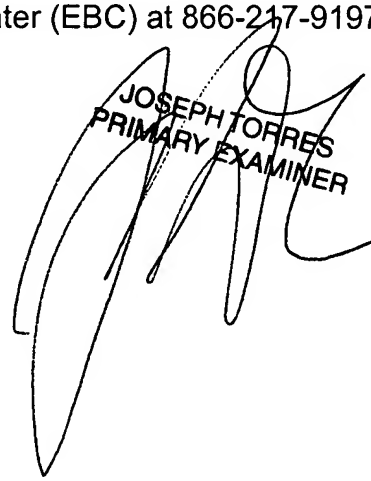
Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (571) 272-3829. The examiner can normally be reached on M-F 8-5.
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Joseph D. Torres, PhD
Primary Examiner
Art Unit 2133